Abstract of the Disclosure

A semiconductor memory device minimizes a data accessing time. For the purpose, it includes a first control signal generator for producing a first control signal by logically combining a pipelatch-in signal and a start-odd start-even data output control signal, a second control signal generator for producing an odd control signal by logically combining an odd data enable signal for outputting odd-numbered data and a control signal for accessing the odd-numbered data in response to a start address, and generating an even control signal by logically combining an even data enable signal for outputting even-numbered data and a control signal for accessing the even-numbered data in response to the start address, a first accessing unit for accessing input data in response to the first control signal, a latch for temporarily storing data outputted from the first data accessing unit, and a second accessing unit for secondly accessing the data stored at the latch, thereby outputting secondly accessed data.